UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,574	10/01/2003	Kenneth M. Carson	APLE.P0063	9303

62224 7590 09/26/2008
ADELI & TOLLEN, LLP
1875 CENTURY PARK EAST
SUITE 1360
LOS ANGELES, CA 90067

EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	
MAIL DATE	**DELIVERY MODE**
09/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,574	CARSON ET AL.	
	Examiner	**Art Unit**	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _24 June 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-8,10,11,13-15,17,18,20-38,40-42 and 44-51_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,2,4-6,8,10,11,13-15,17,18,20-29,31-35,37,38,40-42,44-47 and 49-51_ is/are rejected.

7)☒ Claim(s) _3,7,30,36 and 48_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see p. 15, filed June 24, 2008, with respect to objection to Claim 10 have been fully considered and are persuasive. Objection to Claim 10 has been withdrawn.

2. Applicant's arguments, see p. 16-25, filed June 24, 2008, with respect to the rejection(s) of claim(s) 1 and 34 under 35 U.S.C. 102(e) and claims 2, 4-6, 8, 10, 11, 13-15, 17, 18, 20-25, 35, 37, 38, 40-42, 44, 50, and 51 under 35 U.S.C. 103(a) have been considered and are persuasive. So, rejection has been withdrawn. But, upon further consideration, a new ground(s) of rejection is made in view of Klein (US006738895B1) and Boland (US006269390B1).

3. As per Claims 1, 34, and 35, Applicant argues that Baldwin (US006798421B2) specifies executing its operations using two separate memories instead of using a single cache where the execution does not involve access to other memories (p. 16-17).

In reply, the Examiner has made new grounds of rejection in view of Klein to more clearly teach these limitations.

4. As per Claim 4, Applicant argues Brown (US007006101B1) teaches effect produced by instructions of conditional branch instruction is different. One branch is for ambient light effect and other branch is for non-ambient light effect. So, initial list of routines does not produce same effect as the modified list of routines (p. 19-20). As per Claim 14, Recker (US005657478A) does not disclose modifying the list of routine identifiers by grouping the sendable routine identifiers into at least one set of successive sendable routine identifiers (p. 23-24).

Examiner agrees. However, new grounds of rejection are made in view of Boland.

5. As per Claim 14, Applicant argues that Emer (US006470443B1) does not disclose rearranging instructions for processing by a second processor. Emer recites executing instructions out of order. Accordingly, there is no modified list whereby sendable routine identifiers are grouped together into a set of successive sendable routine identifiers (p. 24).

In reply, Examiner points out new grounds of rejection are made in view of Boland to more clearly teach rearranging routines for processing by second processor and modified list whereby sendable routines are grouped together into a set of successive sendable routines (c. 2, ll. 54-67; c. 3, ll. 1-4, 61-67; c. 4, ll. 6-24; c. 6, ll. 60-65), as discussed below in rejection for Claim 14. Emer teaches rearranging order of fetched instructions, this rearranged order of fetched instruction includes sendable routine identifier since this rearranged order of fetched instruction is sent to be executed (c. 4, ll. 1-10). Emer's teaching of sendable routine identifier can be implemented into Boland's method of rearranging routines for processing by second processor so that Boland's sendable routines are have sendable routine identifiers so sendable routine identifiers are grouped together into a set of successive sendable routine identifiers.

6. Applicant's arguments filed June 24, 2008, with respect to Claims 26-29, 31-33, 45-47, and 49 have been considered but are not persuasive. Applicant argues these claims were rejected along similar or same rationale as Claim 1, and therefore are patentable over Baldwin (p. 17-18).

In reply, Examiner points out these claims were not amended to recite that executing of the passes is performed using the particular cache without accessing other memories outside the processor, and therefore Baldwin still reads on the limitations as the are recited in these claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 27, 28, 32, 46, and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Baldwin (US006798421B2).

9. As per Claims 27 and 46, Baldwin teaches method of executing set of at least two image processing routines on processor using particular cache (c. 18, ll. 11-35), each routine in set of routines processing at least frame of video data (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-46), method comprising determining size of band of frame of video data, wherein frame of video data is divisible into at least two bands (c. 18, ll. 46-59; c. 5, ll. 21-31); and executing set of at least two routines in at least two passes, pass of set of routines comprising each routine in set of routines processing plurality of bands referenced by routine and retrieved from particular cache, in order to produce output data stored to particular cache (c. 18, ll. 5-35).

10. As per Claims 28 and 47, Baldwin teaches determining size of band based on size of cache (c. 18, ll. 46-59; c. 5, ll. 21-31).

11. As per Claim 32, Baldwin teaches plurality of bands retrieved from cache are associated with single frame of video data (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-46).

Thus, it reasonably appears that Baldwin describes or discloses every element of Claims 27, 28, 32, 46, and 47 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B2) and Klein (US006738895B1).

15. As per Claim 1, Baldwin teaches method of executing set of at least two image processing routines on processor using particular cache (c. 18, ll. 11-35), each routine in set of routines processing at least source, each source being frame of video data (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-46), method comprising determining size of band (tile) of source based on size of particular cache, wherein source is divisible into at least two bands (c. 18, ll. 46-59; c. 5, ll. 21-31) and executing set of at least two routines in at least two passes, a pass of set of routines comprising each routine in set of routines processing single band retrieved from particular cache to produce output data stored to particular cache (c. 18, ll. 5-35).

But, Baldwin teaches executing of passes is performed using particular cache and register file present in SIMD element, so, Baldwin does not teach executing of passes is performed using the particular cache without accessing other memories outside processor. But, Klein teaches being able to directly read and write data from/to cache without registers (c. 6, ll. 24-30). So, this teaching from Klein can be implemented into Baldwin so executing of passes is performed using the particular cache without accessing other registers and memories outside processor.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Baldwin so executing of passes is performed using the particular cache without accessing other memories outside processor because Klein suggests that this maximizes the data processing capabilities while reducing power and space requirements (c. 6, ll. 24-44).

16. As per Claim 34, Claim 34 is similar in scope to Claim 1, except that Claim 34 is for computer-readable medium that stores computer program comprising executable code, computer program for performing method of Claim 1. Examiner makes note that computer-readable medium that stores computer program is considered to be read-only- memory (ROM) 820, permanent storage device 825, or system memory 815 as described in Applicant's disclosure on p. 28, ll. 20-p. 29, ll. 8. So, Claim 34 is considered to be directed to statutory subject matter. Baldwin teaches computer-readable medium that stores computer program comprising executable code, computer program for performing method (c. 18, ll. 1-4). So, Claim 34 is rejected under the same rationale as Claim 1.

17. Claims 2, 23, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B2) and Klein (US006738895B1) in view of Karlov (US006958757B2).

18. As per Claims 2 and 35, Baldwin and Klein are relied on for teachings for Claim 1.

But, Baldwin and Klein do not teach determining size of band of sources so all source data processed by and all output data produced by any routine in set of routines can be stored to cache during single processing pass of routine. But, Karlov teaches this (c. 12, ll. 19-26).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Baldwin and Klein to include determining size of band of sources so all source data processed by and all output data produced by any routine in set of routines can be stored to cache during single processing pass of routine because Karlov suggests advantage of using full capacity of cache to drastically reduce the number of cache loads which increases speed (c. 1, ll. 38-67; c. 11, ll. 49-54, 65-67; c. 12, ll. 39-54).

19. As per Claim 23, Baldwin does not teach executing set of at least 2 routines comprises processing of plurality of bands during single pass, each band is associated with separate source. But, Karlov teaches this (c. 12, ll. 19-37; c. 13, ll. 8-21). This is obvious for reasons for Claim 2.

20. Claims 4, 5, 8, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B2), Boland (US006269390B1), and Emer (US006470443B1).

21. As per Claim 4, Baldwin teaches processing plurality of image processing routines on processor using cache (c. 18, ll. 11-35), each routine in plurality of routines processing at least one frame of video data (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-46); and storing output of the routines to a computer-readable medium (c. 18, ll. 30-33).

However, Baldwin does not teach determining initial list comprising plurality of routines positioned in specific order; grouping at least two routines; and modifying initial list of routines to indicate grouping of at least two routines to produce modified list of routines, grouping and modifying are performed by set of instructions executed by processor; executing routines in modified list of routines by traversing modified list of routines. But, Boland teaches method of processing plurality of processing routines on processor using cache (*assigning processes to processors and cache memories associated with each processor,* c. 2, ll. 45-49), method comprising determining initial list comprising plurality of processing routines positioned in specific order which when executed according to specific order produce particular effect (*scheduler 22 schedules all runnable processes in global run queue 24, these processes may thereafter be reordered*, c. 3, ll. 61-67). Boland teaches grouping at least two routines of plurality of routines into set of routines that will run on same processor (c. 4, ll. 6-24). Then these routines will no longer be parallelized or scheduled to run at same time, but these routines will now be serialized on same processor (c. 6, ll. 60-65). So, ordering of routines is modified from parallel ordering to serialized ordering on same processor. So, Boland teaches modifying initial list of routines to indicate grouping of at least two routines to produce modified ordering of initial list of routines (c. 4, ll. 6-24; c. 6, ll. 60-65). Routines which update common data pages are detected by adding code to database's buffer handling routines (c. 5, ll. 41-43), so routines which update common data pages are grouped together to be run serially on same processor (c. 4, ll. 6-24; c. 6, ll. 60-65). So grouping and modifying are performed by code or set of instructions executed by processor (c. 5, ll. 41-43; c. 4, ll. 6-24; c. 6, ll. 60-65). Routines are simply reordered so routines that modify same data pages are running serially on same processor (c. 4, ll. 6-24; c. 6, ll. 60-65), so modified ordering of routines produces the same particular effect as initial list of routines. So, Boland teaches executing routines in modified ordering of routines by traversing modified list of routines to produce the particular effect (c. 4, ll. 6-24; c. 6, ll. 60-65).

It would have been obvious to one of ordinary skill in the art at time of invention to modify Baldwin to include determining initial list comprising plurality of routines positioned in specific order; grouping at least two routines; and modifying initial list of routines to indicate grouping of at least two routines to produce modified list of routines, grouping and modifying are performed by set of instructions executed by processor; executing routines in modified list of routines by traversing modified list of routines because Boland suggests the ordering the routines in such a way as to have fast access to common data, and reduction of lock contention because the routines are ordered in such a way so that various processors do not simultaneously contend for the same lock cell to be able to update the data page (c. 4, ll. 52-60).

However, Baldwin and Boland do not teach routines are identified by routine identifiers. However, Emer teaches method of processing plurality of processing instructions on processor (12, Fig. 1) using cache (13) (c. 3, ll. 39-42; c. 3, ll. 44-46), comprising a) determining initial list of instruction identifiers comprised of plurality of instruction identifiers positioned in specific order, plurality of instruction identifiers identifying plurality of processing instructions, each instruction identifiers in plurality of instruction identifiers identifying corresponding instruction in plurality of instructions (c. 4, ll. 1-6, 16-17); b) grouping at least two instruction identifiers of plurality of instruction identifiers into set of instruction identifiers that identify set of instructions; c) modifying initial list of instruction identifiers to indicate grouping of at least two instruction identifiers to produce modified list of instruction identifiers (c. 1, ll. 18-25; c. 4, ll. 1-10, 60-63); and executing routines identified in modified list of routine identifiers by traversing modified list of routine identifiers. Since Emer teaches changing execution ordering of list of routine identifiers, and execution ordering is considered to be list of routine identifiers, Emer is considered to teach modifying list of routine identifiers. Since Emer teaches altering resources needed by instruction, this means instruction is modified. Since instruction is in list of instructions and instruction is modified, this means list of instructions is modified. By combining Boland's teaching of grouping routines and Emer's teaching of grouping instruction identifiers, it would be obvious to modify Brown to include routine identifiers.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Baldwin and Boland so routines are identified by routine identifiers because Emer suggests using instruction identifiers has advantage of being able to easily distinguish one instruction from another (c. 4, ll. 32-35).

22. As per Claim 5, Baldwin teaches determining size of band of frames of video data of set of routines, each frame of video data having of at least 2 bands where size of band is related to size of cache (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-49; c. 5, ll. 21-31); executing routines identified comprises executing identified routines in 2 or more passes, pass of set of routines comprising each routine in set of routines performing single processing pass where routine processes at least one band retrieved from cache to produce output data stored to cache (c. 18, ll. 5-35).

However, Baldwin does not teach executing routines identified in modified list of routine identifiers. However, Boland teaches executing the routines in modified list of routines (c. 4, ll. 6-24; c. 6, ll. 60-65). This would be obvious for reasons given for Claim 4.

However, Baldwin and Boland do not teach routines are identified by routine identifiers. However, the combination of Emer and Boland teaches this, as discussed for Claim 4.

23. As per Claim 8, Baldwin does not teach re-ordering position of particular routine in initial list of routines to produce set of routines; step c) comprises modifying initial list of

routines to indicate re-ordering of particular routine to produce modified list of routines. But, Boland teaches this limitation (c. 3, ll. 61-67; c. 4, ll. 6-24; c. 6, ll. 60-65). This would be obvious for the same reasons given in the rejection for Claim 4.

However, Baldwin and Boland do not teach routines are identified by routine identifiers. However, Emer teaches step b) further comprises re-ordering position of particular instruction identifier in initial list of instruction identifiers to produce set of instruction identifiers; and step c) further comprises modifying initial list of instruction identifiers to indicate re-ordering of particular instruction identifier to produce modified list of instruction identifiers (c. 1, ll. 18-25; c. 4, ll. 1-10, 60-63). By combining Boland's teaching of grouping routines and Emer's teaching of grouping instruction identifiers, it would be obvious to modify Boland to include routine identifiers. This would be obvious for the same reasons given for Claim 4.

24. As per Claim 24, Boland teaches grouping at least two routines comprises identifying set of at least two routines in modified list of routines that are combinable into single routine for processing on single processor, single routine being capable of performing each routine in set of routines (c. 4, ll. 6-24; c. 6, ll. 60-65).

But, Boland doesn't teach routines are identified by routine identifiers, determining single routine identifier that identifies single routine. But, Emer teaches instructions are fetched from initial list of instructions (c. 4, ll. 1-6). Each instruction is provided with unique instruction identifier (c. 4, ll. 16-17). So, Emer teaches b) identifying set of two or more instruction identifiers in initial list of instruction identifiers that identify set of two or more instructions that are combinable into single instruction, single instruction being capable of performing each instruction in set of instructions; c) determining single instruction identifier that identifiers single instruction (c. 1, ll. 18-25; c. 4, ll. 1-10; c. 4, ll. 60-63). By implementing Emer's teaching of instruction identifiers into Boland's method of processing routines, it would be obvious to modify Boland to include routine identifiers. This would be obvious for reasons for Claim 10.

25. Claims 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B2), Boland (US006269390B1), and Emer (US006470443B1) in view of Karlov (US006958757B2).

26. As per Claim 6, Baldwin, Boland, and Emer are relied on for teachings for to Claim 5.

However, Baldwin, Boland, and Emer do not teach step d) comprises determining size of band of frames of video data so all source data processed by and all output data produced by any routine in set of routines can be stored to cache during single processing pass of routine. But, Karlov teaches this limitation (c. 12, ll. 19-26). This would be obvious for reasons for Claim 2.

27. As per Claim 25, Boland teaches executing the routines identified in the modified list of routine identifiers, as discussed in the rejection for Claim 4.

However, Baldwin, Boland, and Emer do not teach processing a plurality of bands during a single pass, wherein each band is associated with a separate source. But, Karlov teaches this (c. 12, ll. 19-37; c. 13, ll. 8-21). This would be obvious for reasons for Claim 2.

28. Claims 10, 11, 14, 37, 38, 41, 50, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boland (US006269390B1) and Emer (US006470443B1).

29. As per Claim 10, Boland teaches method of processing plurality of routines, method comprising determining initial list comprising plurality of routines which when executed produce particular effect (c. 3, ll. 61-67); identifying set of at least two routines in initial list of routines that are combinable into single routine for processing in single processor, single routine being

capable of performing each routine in set of routines, at least one routine in set of routines comprises plurality of instructions; single routine is intended to produce the particular effect when executed with other routines that were not identified as combinable into single routine, identifying of set of at least two routines and determining of single routine are performed by set of instructions executed by processor (c. 4, ll. 6-24; c. 6, ll. 41-43; c. 6, ll. 60-65). Single routine is sent to processor for execution by processor (c. 4, ll. 6-24; c. 6, ll. 41-43). So, it would be obvious to one of ordinary skill in the art that single routine is stored to computer-readable medium within processor so processor can execute single routine.

But, Boland does not teach routines are identified by routine identifiers, determining single routine identifier that identifiers single routine, determining of single routine identifier is performed by set of instructions executed by processor; storing single routine identifier to computer-readable medium. But, Emer teaches instructions are fetched from initial list of instructions (c. 4, ll. 1-6). Each instruction is provided with unique instruction identifier (c. 4, ll. 16-17). So, Emer teaches processing plurality of instructions, a) determining initial list of routine identifiers comprised of plurality of instruction identifiers identifying plurality of instructions, each instruction identifier in plurality of instruction identifiers identifying corresponding routine in plurality of instructions (c. 4, ll. 1-6, 16-17); b) identifying set of at least 2 instruction identifiers in initial list of instruction identifiers that identify set of at least 2 instructions that are combinable into single instruction, single instruction being capable of performing each instruction in set of instructions; c) determining single instruction identifier that identifiers single instruction, determining of single instruction identifier is performed by set of instructions executed by processor; storing single routine identifier to computer-readable medium (c. 1, ll.

18-25; c. 4, ll. 1-10; c. 4, ll. 60-63). Emer teaches fetching up to 8 instructions per cycle (c. 4, ll. 1-6), result of each of fetches is merged before instructions are executed (c. 4, ll. 9-10). Since fetched instructions are merged before being executed, this means instructions are combined into single instruction. Emer teaches **during fetch**, each instruction is provided with unique instruction identifier (c. 4, ll. 16-17). Result of each of fetches is merged before instructions are executed (c. 4, ll. 9-10). Instructions are combined into single instruction queue (c. 4, ll. 60-63). So, **at time** of fetch, each instruction has unique instruction identifier, but **after** fetching and merging, single routine identifier identifies routines in initial list of routine identifiers. By implementing Emer's teaching of instruction identifiers into Boland's method off processing routines, it would be obvious to modify Boland to include routine identifiers.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Boland so routines are identified by routine identifiers and determining single routine identifier that identifiers single routine because Emer suggests being able to group together routines that are not dependent upon other instructions in instruction stream, and also selecting more suitable threads to be grouped together, so resulting in higher performance processor (c. 1, ll. 18-25; c. 2, ll. 42-45). Emer suggests using instruction identifiers has advantage of being able to easily distinguish one instruction from another (c. 4, ll. 32-35).

30. As per Claim 11, Boland teaches producing modified list of routines; and executing routines identified in modified list of routines (c. 4, ll. 6-24; c. 6, ll. 60-65).

But, Boland does not teach routines are identified by routine identifiers and replacing set of routine identifiers in initial list of routine identifiers with single routine identifier to produce modified list of routine identifiers. But, Emer teaches replacing set of instruction identifiers in initial list of instruction identifiers with single instruction identifier to produce modified list of instruction identifiers; and executing instructions identified in modified list of instruction identifiers (c. 1, ll. 18-25; c. 4, ll. 1-10, 60-63). By implementing Emer's teaching of instruction identifiers into Boland's method of processing routines, it would be obvious to modify Boland to include routine identifiers. This would be obvious for reasons for Claim 10.

31. As per Claims 14 and 41, Boland teaches method of executing plurality of routines for execution by at least first processor, method comprising determining initial list comprising plurality of routines which when executed produce particular effect (c. 3, ll. 61-67); identifying at least two routines in initial list of routines as sendable routines that are able to be processed by second processor; before executing routines in list of routines, modifying list of routines by grouping sendable routines into at least one set of successive sendable routines (c. 4, ll. 6-24; c. 6, ll. 60-65; c. 2, ll. 54-c. 3, ll. 4) that minimize number of transfers for transferring sendable routines from first processor to be processed by second processor (c. 1, ll. 4-9; c. 2, ll. 45-c. 3, ll. 4), identifying of sendable routines and modifying of list of routines are performed by set of instructions executed by first processor; and storing modified list of routines to computer-readable medium for subsequent execution of modified list that is intended to produce the particular effect (c. 5, ll. 41-43; c. 4, ll. 6-24; c. 6, ll. 60-65).

But, Boland does not teach routine identifiers identifying plurality of routines, each routine identifier identifying corresponding routine in routines; before executing routines identified in list of routine identifiers, modifying list of routine identifiers to include sendable routine identifier, modifying of list of routine identifiers is performed by set of instructions executed by 1st processor; d) storing modified list of routine identifiers to computer-readable medium. But, Emer teaches executing plurality of instructions that are able to be executed on first processor (12, Fig. 1; c. 3, ll. 39-42), a) determining initial list of instruction identifiers comprised of plurality of instruction identifiers identifying plurality of instructions, each instruction identifier in plurality of instruction identifiers identifying corresponding routine in plurality of instructions (c. 4, ll. 1-6, 16-17); c) before executing routines identified in list of routine identifiers, modifying list of routine identifiers to include sendable routine identifier, modifying of list of routine identifiers is performed by set of instructions executed by 1st processor; d) storing modified list of routine identifiers to computer-readable medium (c. 4, ll. 1-10, 60-64). Emer teaches rearranging order of fetched instruction, this rearranged order of fetched instruction includes sendable routine identifier since this rearranged order of fetched instruction is sent to be executed (c. 4, ll. 1-10). By implementing Emer's teaching of instruction identifiers into Boland's method of processing routines, it would be obvious to modify Boland to include routine identifiers.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Boland so before executing routines identified in list of routine identifiers, modifying list of routine identifiers to include sendable routine identifier because Emer suggests selecting preferred routines before executing routines in order to prevent execution of routines that are not needed, so increasing execution speed (c. 2, ll. 25-65). It would have been obvious to include routine identifiers identifying plurality of routines, each routine identifier identifying corresponding routine in routines for reasons for Claim 4.

32. As per Claims 37 and 38, these claims are similar in scope to Claims 10 and 11 respectively, and therefore are rejected under the same rationale.

33. As per Claim 50, Boland does not teach using modified list of routine identifiers to direct first processor to execute plurality of routines. However, Emer teaches this limitation (c. 3, ll. 64-c. 4, ll. 10). This would be obvious for the same reasons given in the rejection for Claim 14.

34. As per Claim 51, Boland does not teach set of instructions for executing plurality of routines using modified list of routine identifiers. But, Emer teaches this (c. 3, ll. 51-57; c. 4, ll. 1-10; c. 5, ll. 38-39, 66-67; c. 6, ll. 1-3). This would be obvious for reasons for Claim 14.

35. Claims 13, 21, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boland (US006269390B1) and Emer (US006470443B1) in view of Dawson (US004876651A).

Boland and Emer are relied on for teachings for Claim 10. Boland and Emer teach combining at least two routine identifiers into single routine identifier, as discussed for Claim 10.

However, Boland and Emer do not teach identifying routines using look-up table. However, Dawson teaches identifying routines using look-up table (c. 15, ll. 35-39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Boland and Emer to include identifying routines using look-up table as suggested by Dawson. Look-up tables increase processing speed. Look-up tables are well-known in the art, widely used, and can be found in many publications.

36. Claims 15, 17, 18, 22, 42, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boland (US006269390B1) and Emer (US006470443B1) in view of Ngai (US006995770B2).

37. As per Claims 15 and 42, Boland teaches sending sendable routine to alternative processor for processing and then receives data produced by sendable routine; modifying initial list of routines to indicate replacing of sendable routine to produce modified list of routines; and

method comprises executing routines identified in modified list of routines (c. 2, ll. 54-c. 3, ll. 4; c. 4, ll. 6-24; c. 6, ll. 60-65). Combination of Emer and Boland teaches routine identifiers identifying plurality of routines, each routine identifier identifying corresponding routine in routines, as discussed for Claim 14.

But, Boland and Emer do not teach replacing sendable routine identifier in initial list of routine identifiers with “alternative processor” routine identifier that identifies “alternative processor” routine that sends sendable routine to alternative processor for processing. But, Ngai teaches off-loading instructions from CPU to controller (c. 4, ll. 40-42), and for routines that are to be executed by alternative processor, controller identifies these routines by “alternative processor” routine identifier (c. 1, ll. 48-56, c. 4, ll. 40-55). Since these routines are off-loaded from CPU, Ngai inherently teaches replacing sendable routine identifier in initial list of routine identifiers with “alternative processor” routine identifier that identifies “alternative processor” routine that sends sendable routine to alternative processor for processing.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Boland and Emer to include “alternative processor” routine identifier because Ngai teaches knowing which processor routine needs to be sent to (c. 4, ll. 40-55).

38. As per Claims 17 and 44, these claims are each is similar in scope to Claim 15, except that Claims 17 and 44 are for successive sendable routines. Boland teaches successive sendable routines (c. 2, ll. 54-c. 3, ll. 4; c. 4, ll. 6-24; c. 6, ll. 60-65). Therefore Claims 17 and 44 and rejected under the same rationale as Claim 15.

39. As per Claim 18, Boland teaches modifying initial list of routines comprises modifying initial list of routines to indicate re-ordering of identified routines to produce modified list of routines (c. 4, ll. 6-24; c. 6, ll. 60-65).

However, Boland does not teach modifying initial list of routine identifiers comprises modifying initial list of routine identifiers to indicate re-ordering of identified routine identifiers to produce modified list of routine identifiers. But, Emer teaches grouping at least 2 sendable instruction identifiers has re-ordering position of particular instruction identifier in initial list of instruction identifiers to produce set of instruction identifiers; modifying initial list of instruction identifiers has modifying initial list of instruction identifiers to indicate re-ordering of the identified instruction identifiers to produce modified list of instruction identifiers (c. 1, ll. 18-25; c. 4, ll. 1-10, 60-63). By implementing Emer's teaching of instruction identifiers into Boland's method of processing routines, it would be obvious to modify Boland to include routine identifiers. This would be obvious for reasons for Claim 10.

40. As per Claim 22, Boland teaches further comprising having the alternative processor process the sendable routine; receiving processed data from the alternative processor (c. 2, ll. 54-c. 3, ll. 4; c. 4, ll. 6-24; c. 6, ll. 60-65).

41. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boland (US006269390B1) and Emer (US006470443B1) in view of Recker (US005657478A).

Boland and Emer are relied upon for teachings as discussed above relative to Claim 14.

However, Boland and Emer do not teach that the first processor is a CPU and the second processor is a graphics processor. However, Recker teaches 1st processor (10) is CPU and 2nd processor is graphics processor (30) (c. 1, ll. 42-55; c. 3, ll. 1-15).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Boland and Emer so that the first processor is a CPU and the second processor is a graphics processor because Recker suggests that it is advantageous for a CPU to selectively offload commands to a graphics processor in order to achieve efficiency and flexibility without incurring tearing effects of the display (c. 1, ll. 28-33, 42-61; c. 2, ll. 2-5).

42. Claims 26 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B1) and Emberling (US006933945B2).

Baldwin teaches executing set of at least 2 image processing routines on processor using cache (c. 18, ll. 11-35), each routine in set of routines processing frame of video data (c. 1, ll. 63-c. 2, ll. 9; c. 18, ll. 43-46), determining size of band of frame of video data based on size of cache, frame of video data is divisible into at least 2 bands (c. 18, ll. 46-59; c. 5, ll. 21-31); executing set of at least 2 routines in at least 2 passes, pass of set of routines having each routine in set of routines processing single band retrieved from cache to produce output data stored to cache (c. 18, ll. 5-35).

But, Baldwin doesn't teach determining size of band based on buffers referenced by routine in cache. But, Emberling teaches determining size of band of frame based on plurality of buffers (bin scan line memories) referenced by routine in cache (c. 15, ll. 20-32, 50-58).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Baldwin to include determining size of band based on buffers referenced by routine in cache because Emberling teaches there needs to be enough space in buffers to hold data pertaining to band (c. 15, ll. 20-32).

43. Claims 29, 31, 33, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin (US006798421B1) in view of Karlov (US006958757B2).

As per Claim 29, Claim 29 is similar in scope to Claim 2, and therefore is rejected under the same rationale. As per Claims 31, 33, and 49, these claims are each similar in scope to claim 23, and therefore are rejected under the same rationale.

Allowable Subject Matter

44. Claims 3, 7, 30, 36, 48 are objected to as being dependent on rejected claim, but would be allowable if rewritten in independent form including limitations of base and intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of advisory action. In no event, however, will statutory period for reply expire later than SIX MONTHS from date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628